REMARKS

In this paper, we amended various claims and added others. At present, the application contains claims 4-5, 7-12, and 19-23.

RESTRICTION REQUIREMENT

Non-elected claims 1-3 and 13-18 have been canceled in accordance with a previous restriction requirement.

35 USC 112 REJECTIONS

The office action objected to claims 4-5, 7-9, and 12 under 35 USC 112, second paragraph. The claims (as amended) fully comply with section 112. The claim amendments are well supported in the original disclosure. Accordingly, we have not added any new matter.

ALLOWABLE SUBJECT MATTER

Claim 11 has been allowed. Claim 12 was cited as being allowable subject to being rewritten as an independent claim and having the section 112 issue (mentioned above) overcome. Claim 12 does not need to be written, however, since the rejections to base claim 4 have been overcome (as discussed below).

35 USC 103 REJECTIONS: GRUNDMANN

The office action rejected claims 4-5, 7-9 under 35 USC 103 as being unpatentable over Grundmann in view of one or more of McElvain or Duggirala or Cooke. The exact patent and publication numbers are these and any later-cited references are already stated the record. These claims are patentably distinguished from the applied art, as explained below.

Taking claim 4 as an example, the applied references do not teach "**replacing flip-flops in said digital circuit with negative delay elements**." Grundmann refers to the replacement of a flip-flop 100 with logically equivalent elements comprising a multiplexer 110 coupled to a latency delay unit 105. [Fig.

1B] As to Grundmann's purported logically equivalent element, further study reveals that Fig. 1A and Fig. 2A are actually not logically equivalent. Indeed, a logic equivalence verification tool would complain upon encountering such a transformation. At any rate, these logically equivalent elements do not constitute a negative delay element. So, in this operation, Grundmann is not replacing a flip-flop with a negative delay element as claimed.

Elsewhere, Grundmann does mentions various "latency delay units" with a delay of "-1." [Col. 4, lines 55 – col. 5, line 10; Claim 6; Figs. 3A, 4C, 5] However, the above-mentioned flip-flop replacement operation and the operations using negative delay elements are completely unrelated. Indeed, in using the (-1) latency delay units, Grundmann ultimately seeks to eliminate latency delay, "since the latency delay unit having a latency delay of -1 unit cancels the latency delay unit 325 having a latency delay of +1 unit." And, a new latency delay unit 345 is added to the output of function F to represent the +1 latency delay unit added in the feedback loop. Thus, Grundmann does not show replacing flip-flops in said digital circuit with negative delay units, as claimed. For this reason, claim 4 is distinguished from Grundmann.

Claim 4 is further patentable because the references do not show "**breaking any feedback paths in the digital circuit by inserting dummy flip-flops clocked by clocks all having an infinitesimal period**. " Although Grundmann at one point is said to form a "logically redundant element" (e.g., ref. 150, Fig. 1E), he does not disclose breaking a feedback loop with this element. Instead, Grundmann bypasses the FSM register using his logically redundant element. Furthermore, Grundmann's bypassing (e.g., Figs. 2A-2B) creates a combination loop (from F to 225 to 235 to F again), which renders this circuit invalid for use in the context of "a method for generating timing constraints" as claimed. Grundmann's disclosure fails recognize this newly created combinational loop, or show how to break it. Accordingly, Grundmann does not break feedback paths in the digital circuit as claimed.

Moreover, Grundmann never suggests breaking feedback paths using a dummy flip-flop clocked with an infinitely small period, as claimed. Instead,

Grundmann's logically redundant element is formed by a select line of a multiplexer to the enable input of a conditional state element. The dummy flip-flop, clocked as claimed, is missing from Grundmann.

By the foregoing examples, claim 4 is distinguished from Grundmann. And none of McElvain or Duggirala or Cooke provide the features missing from Grundmann. The office action introduced these references merely to add an HDL context. [Office Action, page 3]

Even without considering the individual merits of dependent claims 5, 7-9, these are distinguished over the applied art for the reasons stated above, because they depend from claim 4.

35 USC 103 REJECTIONS: LABERGE

The office action rejected claim 10 as being unpatentable over Laberge in view of one or more of McElvain or Duggirala or Cooke. Claim 10 is patentable because the applied art does not teach the claimed features.

For instance, Laberge does not teach the claimed a step of "replacing flip-flops in said digital circuit with negative delay elements." The office action identified Figure 4 as showing buffers (tree) with negative delay elements. However, a closer review of the figure and text reveals that each of Laberge's gates is said to have a propagation delay value associated with it, determined from a previous timing analysis of the gate. For example, the AND gate 406 has a propagation delay of 0.5 nanoseconds. Other illustrated gates have propagation delays of 1.0, 0.5, 1.5, and 0.5 nanoseconds. In no case is there any discussion, however, of a negative delay. Accordingly, Laberge does not contemplate any negative delay elements. Hence, Laberge fails to show "replacing flip-flops in said digital circuit with negative delay elements" as claimed.

Nor does Laberge teach "where some of the negative delay elements comprise buffers, said buffers having a load capacitance representing an average or weighted-average load capacitance taken over inputs of all gates and flip-flop D pins in a target technology library." Laberge only mentions

capacitance three times, and then only in a vague manner. The office action did not identify any specific teaching of Laberge related to the foregoing feature.

NEW CLAIMS

We have added claims 19-23 to the application. All claims are supported by the originally filed specification and drawings. No new matter has been added.

New claims 20 adds a "step for" claim to the application, similar to existing independent claim 1. New claims 21-22 add computer program product claim counterparts to claims 4 and 11, New claim 23 adds a system claim counterpart to claim 4. The present disclosure describes various computer implemented methodologies, and the embodiment of such technology in forms such as computer storage products or a computer driven system is abundantly evident to ordinarily skilled artisans without further explanation.

REQUEST FOR FURTHER EXPLANATION

The office action took the approach of copying Applicant's claim language verbatim and annotating it with brief citations to the drawings of Grundmann and Laberge. However, in many cases, the Figures did not seem to be applicable, and the office action did not explain any of its reasoning. In the interest of efficiency, we kindly request direct, explanatory, and specific citations from the text of the reference, along with some clear explanation of the Examiner's reasoning.

The Supreme Court has recently made some useful observations as to obviousness that, by analogy, apply equally to rejections under 35 USC 102. For instance, the Court has emphasized that rejections "cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning."[1] The Court also required the analysis supporting a rejection to be made "explicit.[2] The Court specifically confirmed that this analysis

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1 KSR Int'l Co. v. Teleflex, 127 S.Ct. 1727, 1741 (2007).
2 Id.

is equally applicable to the courts and patent examiners.[3]

Relatedly, it is important for an examiner to properly communicate the basis for a rejection so that the issues can be identified early and the applicant can be given fair opportunity to reply. MPEP 706.02(j)

CONCLUSION

In view of the foregoing, all pending claims in the application are patentable over the applied art. We request favorable reconsideration and allowance of all claims in the application.

FEES

The Commissioner is authorized to charge any fees due to the Glenn Patent Group Deposit Account No. 07-1445, Customer No. 22862.

Respectfully Submitted,

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3 Id. at 1734.